CPRE 4910 Weekly Report 05

10/21/2025 - 10/27/2025

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Validation Lead***
Dawud Benedict	***-Toolflow Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**

  During the Advisor meeting, we found that OpenRAM would fail DRC checks at the foundry. We also worked on integrating our existing modules into the top-level design file with firmware.

- **Past Week Accomplishments**

  - Colin McGann: Working on integrating the VGA and rasterizer together. Fixing bugs with the VGA and memory controllers. Still making optimizations on the rasterizer.
  - Jack Tonn: Sent in picture/bio for website, refined SVUnit testing framework and tutorial, created and presented the plus delta team reflection
  - Dawud Benedict: Testing Precheck with Sky130 PDK .gds and .lef output by Cadence. Contacted Cadence to get PDK documentation. Continued Wishbone-PKBus bridge.
  - Michael Drobot: Started and finished Wishbone config register module, used for memory-mapping our modules to the management core. Familiarized myself with

the Wishbone bus spec and how the management core addresses the user area. Dropped OpenRAM after talking to Dr. Duwe, he said it likely won't pass DRC at the fab.

- Sam Forde: Sent in bio/pic for website. Worked through integrating Verilog mac into Caravel for testing purposes.
- Josh Arceo: Finished a rudimentary fragment shader c code sample
- Emil Kosic: Familiarization of vertex shading architecture, improving vertex shader implementation code to take in a custom image and output values needed for working rasterizer to test against.

- **Pending Issues**
  - Confirm Cadence tools will work for tapeout.
  - Fix VGA module hardening issues.

- **Individual contributions**

NAME	Individual Contributions	Hours this week	HOURS cumulative
Colin McGann	Integrating VGA and memory system. Rsaterizer optimizations.	15	80
Jack Tonn	Refined SVUnit testing framework & plus-delta team reflection	4	34
Dawud Benedict	Sky130 PDK Cadance, Continued HDL	5	32
Michael Drobot	Wishbone config register, management core integration	10	50
Sam Forde	Worked on integrating Verilog into Caravel for testing purposes.	6	32
Josh Arceo	Fragment shader C code	4	24
Emil Kosic	Vertex Shader code, ISA research	5	26

- **Plans for the upcoming week**
  - Colin McGann: Continue debugging the VGA and memory so that we have something cool to show off for our advisor meeting.
  - Jack Tonn: Teach verification flow, work with ISA group to develop the cores
  - Dawud Benedict: Continue HDL, start new module – discuss details during the Advisor/Client meeting.

- Michael Drobot: Work on integrating VGA into the top-level design. Test VGA, memory, PKBus, and management core together. Start on firmware.
- Sam Forde: Continue working on getting design into Caravel. Discuss next tasks to work on with group if everything is wrapped up this week.
- Josh Arceo: Assist with ISA so that we can convert from C code to assembly
- Emil Kosic: Continue ISA research and begin designing cores

- **<u>Advisor Meeting Summary</u>**

In our meeting, we presented our plus-delta team reflection, as seen below.

	Plus	Delta (progress)	Delta (understanding)
Technical	Designed the architecture of the uGPU	Write Verilog & SVUnit test bench	Give presentations on design & document design choices and reasons
Economic	We only have one option of company to work with, and we cannot change the price of production	Little to none can be done to change the economic price of this product	We could research and reach out to companies with more competitive pricing
Human	Defined users/user groups, built design to support those users	Explain why we have selected these user groups	Research our user groups potentially interview these users

Our advisor suggested that we could explore the economic impact of the product more, and instead of just thinking about the economic impact on us for producing the uGPU, we could instead focus on the impact on our user groups, and how this product will help them acquire GPUs. Thus, we will continue to explore the impact of our product, and we will assign someone to ensure that our design decisions are driven by our users and our own opinions, instead of just our opinions.